UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,591	07/16/2003	**Shih-Hsien Wu**	TAIW 813	7448

23995 7590 01/29/2010

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
01/29/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/619,591	WU ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-41,43-53 and 55-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-41,43-53 and 55-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37-41, 43-53 and 55-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh et al. in view of Nishide et al. (5,827,605).

Regarding claims 37-38, Satoh et al. teach in figure 11 and related text a composite laminated substrate for integrated and minimized electronic circuits, comprising:

an inorganic glass substrate 1 having at least one passive component 20 embedded therein; and

an organic substrate 2 which is laminated to one side of the inorganic substrate and which has circuits for electrical connections to the at least one passive component of the inorganic substrate.

Regarding claims 49-50, Satoh et al. teach in figure 11 and related text a composite laminated substrate for integrated and minimized electronic circuits, comprising:

an inorganic substrate 1 having at least one passive component inductor 4 formed thereon or embedded therein; and

two organic substrates 2 which are laminated to respective sides of the inorganic substrate and integrated therewith, and which have circuits for electrical connections to the at least one passive component of the inorganic substrate.
Although element 20 can be considered as a passive element, Satoh et al. do not explicitly state that the inorganic substrate has at least one passive component embedded therein, and does not state that the organic substrate is composed of a plurality of stacked printed circuit boards.
Nishide et al. teach in figure 1 and related text an inorganic substrate 2 having at least one passive component 6 embedded therein.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an inorganic substrate having at least one passive component embedded therein, and to use an organic substrate composed of a plurality of stacked printed circuit boards with each having its own respective separate circuitry, in prior art's device, in order to reduce the size of the device by incorporating passive elements within the inorganic substrate and by stacking a plurality of printed circuit boards, respectively.

Regarding claims 45-47, Satoh et al. teach in figure 11 and related text the organic substrate further comprises at least one passive component, wherein the at least one passive component is selected from the group consisting of a capacitor, an inductor, a resistor and any mixture thereof, and wherein the organic substrate is a built-up organic substrate provided on the inorganic substrate.

Regarding claims 53 and 57-59, Satoh et al. teach in figure 11 and related text at least one of the two organic substrates further comprises at least one passive component, wherein the at least one passive component of the at least one of the two organic substrates is selected from the group consisting of a capacitor, an inductor, a resistor, and any mixture thereof, and wherein at least one of the two organic substrates is a built-up organic substrate provided on the inorganic substrate

Regarding claims 57-59, Satoh et al. teach in figure 11 and related text at least one of the two organic substrates further comprises at least one passive component, wherein the at least one passive component of the at least one of the two organic substrates is selected from the group consisting of a capacitor, an inductor, a resistor, and any mixture thereof, and wherein at least one of the two organic substrates is a built-up organic substrate provided on the inorganic substrate

Regarding claims 39 and 51, Satoh et al. teach the at least one passive component is one of a thick film or thin film passive component, but does not teach using ceramic substrate.
Nishide et al. teach in figure 1 and related text using ceramic substrate 2.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use ceramic substrate in prior art's device in order to form the device of a conventional substrate material, of which official notice is taken.

Regarding claims 40 and 52, Satoh et al. teach the at least one passive component is a semiconductor fabricated passive component, but does not teach using silicon substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use silicon substrate in prior art's device in order to form the device of a conventional substrate material, of which official notice is taken.

Regarding claims 41, 44-47 and 56-59, Satoh et al. teach in figure 11 and related text the at least one passive component is selected from the group consisting of a capacitor, an inductor, a resistor and any mixture thereof, and

the organic substrate further comprises at least one passive component, wherein the at least one passive component is selected from the group consisting of a capacitor, an inductor, a resistor and any mixture thereof, and wherein the organic substrate has an outer surface layer is a built-up surface layer which includes a circuit, and an organic substrate provided on the inorganic substrate.

Regarding claims 42-43 and 54-55, prior art does not explicitly state that the organic substrate is composed of a plurality of stacked printed circuit boards with each having its own respective separate circuitry. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an organic substrate is composed of a plurality of stacked printed circuit board with each having its own

respective separate circuitry in prior art's device in order to reduce the size of the device.

Regarding claims 48 and 61, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a bonding layer which is provided between the inorganic substrate and the organic substrate, and which bonds together the inorganic substrate and the organic substrate in prior art's device, in order to improve the structural integrity of the device.

Regarding claim 60, prior art's device includes a covering layer (the top layer) which is provided on the inorganic substrate and covers the inorganic substrate, which integrates the inorganic substrate with one of the two organic substrates, and which comprises circuits for providing electrical connections between the at least one passive component of the inorganic substrate and said one of the two organic substrates. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to fully cover the inorganic substrate said two organic substrates, in prior art's device, in order to simplify the processing steps of making the device.

Regarding claims 62-63, prior art's device includes the at least one passive component is separated from, so as to not directly contact, the two organic substrates.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37-41, 43-53 and 55-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh et al. in view of Ammon (3,868,162) and Nishide et al. (5,827,605).

Regarding claims 37-38, Satoh et al. teach in figure 11 and related text a composite laminated substrate for integrated and minimized electronic circuits, comprising:

an inorganic glass substrate 1 having at least one passive component 20 embedded therein; and

an organic substrate 2 which is laminated to one side of the inorganic substrate and which has circuits for electrical connections to the at least one passive component of the inorganic substrate.

Regarding claims 49-50, Satoh et al. teach in figure 11 and related text a composite laminated substrate for integrated and minimized electronic circuits, comprising:

an inorganic substrate 1 having at least one passive component inductor 4 formed thereon or embedded therein; and

two organic substrates 2 which are laminated to respective sides of the inorganic substrate and integrated therewith, and which have circuits for electrical connections to the at least one passive component of the inorganic substrate.

Although element 20 can be considered as a passive element, Satoh et al. do not explicitly state that the inorganic substrate has at least one passive component embedded therein, and does not state that the organic substrate is composed of a plurality of stacked printed circuit boards.

Nishide et al. teach in figure 1 and related text an inorganic substrate 2 having at least one passive component 6 embedded therein.

Ammon teaches in figure 1 and related text an organic substrate 13 or 14 composed of a plurality of stacked printed circuit boards with each having its own respective separate circuitry.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an inorganic substrate having at least one passive component embedded therein, and to use an organic substrate composed of a plurality of stacked printed circuit boards with each having its own respective separate circuitry, in prior art's device, in order to reduce the size of the device by incorporating passive elements within the inorganic substrate and by stacking a plurality of printed circuit boards, respectively.

Regarding claims 45-47, Satoh et al. teach in figure 11 and related text the organic substrate further comprises at least one passive component, wherein the at least one passive component is selected from the group consisting of a capacitor, an inductor, a resistor and any mixture thereof, and wherein the organic substrate is a built-up organic substrate provided on the inorganic substrate.

Regarding claims 53 and 57-59, Satoh et al. teach in figure 11 and related text at least one of the two organic substrates further comprises at least one passive component, wherein the at least one passive component of the at least one of the two organic substrates is selected from the group consisting of a capacitor, an inductor, a resistor, and any mixture thereof, and wherein at least one of the two organic substrates is a built-up organic substrate provided on the inorganic substrate

Regarding claims 57-59, Satoh et al. teach in figure 11 and related text at least one of the two organic substrates further comprises at least one passive component, wherein the at least one passive component of the at least one of the two organic substrates is selected from the group consisting of a capacitor, an inductor, a resistor, and any mixture thereof, and wherein at least one of the two organic substrates is a built-up organic substrate provided on the inorganic substrate

Regarding claims 39 and 51, Satoh et al. teach the at least one passive component is one of a thick film or thin film passive component, but does not teach using ceramic substrate.
Nishide et al. teach in figure 1 and related text using ceramic substrate 2.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use ceramic substrate in prior art's device in order to form the device of a conventional substrate material, of which official notice is taken.

Regarding claims 40 and 52, Satoh et al. teach the at least one passive component is a semiconductor fabricated passive component, but does not teach using silicon substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use silicon substrate in prior art's device in order to form the device of a conventional substrate material, of which official notice is taken.

Regarding claims 41, 44-47 and 56-59, Satoh et al. teach in figure 11 and related text the at least one passive component is selected from the group consisting of a capacitor, an inductor, a resistor and any mixture thereof, and

the organic substrate further comprises at least one passive component, wherein the at least one passive component is selected from the group consisting of a capacitor, an inductor, a resistor and any mixture thereof, and wherein the organic substrate has an outer surface layer is a built-up surface layer which includes a circuit, and an organic substrate provided on the inorganic substrate.

Regarding claims 42-43 and 54-55, prior art does not explicitly state that the organic substrate is composed of a plurality of stacked printed circuit boards with each having its own respective separate circuitry. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an organic substrate is composed of a plurality of stacked printed circuit board with each having its own

respective separate circuitry in prior art's device in order to reduce the size of the device.

Regarding claims 48 and 61, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a bonding layer which is provided between the inorganic substrate and the organic substrate, and which bonds together the inorganic substrate and the organic substrate in prior art's device, in order to improve the structural integrity of the device.

Regarding claim 60, prior art's device includes a covering layer (the top layer) which is provided on the inorganic substrate and covers the inorganic substrate, which integrates the inorganic substrate with one of the two organic substrates, and which comprises circuits for providing electrical connections between the at least one passive component of the inorganic substrate and said one of the two organic substrates. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to fully cover the inorganic substrate said two organic substrates, in prior art's device, in order to simplify the processing steps of making the device.

Regarding claims 62-63, prior art's device includes the at least one passive component is separated from, so as to not directly contact, the two organic substrates.

Response to Arguments

Applicant argues that independent claims 37 and 49 are amended to incorporate the contents in claim 42 and claim 54, respectively.

Although the content of dependent claims 42 and 54 was incorporated in independent claims 37 and 49, respectively, the newly presented independent claims 37 and 49 comprise broader limitations that the limitations of previously presented claims 42 and 54, respectively.

Applicant argues that "the through hole 20 in Satoh et al. is not a passive component".

A resistor is a conductor having resistance. A resistor is a passive element. Element 20 is a conductor. A conductor inherently has a resistance. Therefore, element 20 is a passive element.

Applicant argues that "Satoh et al. teach a semiconductor connection substrate which connects a semiconductor element to a mounting substrate such as a printed substrate. It is clear that the substrate in Satoh et al. does not have a printed substrate".

It appears that applicant agrees that Satoh et al. teach a printed substrate.

Applicant argues that "the Examiner has merely provided a specious motivation to combine Satoh et al. and Nishide et al. The Examiner must demonstrate that there would be a motivation to combine Satoh et al. and Nishide et al. However, the Examiner

has merely identified language in the Satoh et al. and Nishide et al. that is, at most, a purported advantage of using these references alone".

The motivation to use an organic substrate composed of a plurality of stacked printed circuit boards with each having its own respective separate circuitry, and to incorporate passive elements within the inorganic substrate in prior art's device is to reduce the size of the device. Ammon is further cited as evidence to teach that it is conventional to form a plurality of stacked printed circuit boards.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
1/28/2010

/ORI NADAV/
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800